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PATENT



## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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C. Healion  
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102800 MAIL ROOM

Applicant : Janardhanan S. Ajit  
Application No. : 10/043,763  
Filed : January 9, 2002  
Title : SUB-MICRON HIGH INPUT VOLTAGE  
TOLERANT INPUT OUTPUT (I/O) CIRCUIT  
WHICH ACCOMMODATES LARGE POWER  
SUPPLY VARIATIONS  
Docket No. : 41980/RJP/B600

### PRELIMINARY AMENDMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Post Office Box 7068  
Pasadena, CA 91109-7068  
July 30, 2002

Commissioner:

#### In the Drawings

Please amend Figures 4, 12A, 12B and 13 as indicated in the amended and formalized drawings enclosed herewith marked in red. Unchanged but formalized drawings are included herewith for the Examiner's reference convenience.

### REMARKS

The Applicant has discovered NMOS versus PMOS circuit depiction errors in certain of the Figures in the above-referenced Application. Corrections have been made to the drawings such that they are consistent with the circuits and their operation as described in the Specification as filed. Accordingly, the Applicant submits that no new matter has been added.

BEST AVAILABLE COPY

Please enter these drawing amendments and take them into consideration when examining the Application.

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

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RJP/cah

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